Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0004	Serial No.: 10/681,577
Information Disclosure Statement by Applicant	Applicant: Christopher J. Diorio et al.	
(Use several sheets if necessary)	Filed: October 7, 2003 Group: 2816	

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
HN	A	2002/0089440	7/11/2002	Kranz et al.	327	112	
	B	3,958,236	5/18/1976	Kelly	341	128	
	C	4,163,947	8/7/1979	Weedon	327	341	
	D	4,914,440	4/3/1990	Ramet	341	140	
	E	5,029,063	7/2/1991	Lingstaedt	363	60	
	F	5,099,156	3/24/1992	Delbruck	327	63	
	G	5,243,347	9/7/1993	Jackson et al.	341	144	
	H	5,332,997	7/26/1994	Dingwall et al.	341	150	
	I	5,376,935	12/27/1994	Seligson	341	136	
	J	5,553,030	9/3/1996	Tedrow et al.	365	226	
	K	5,608,400	3/4/1997	Pellon	341	143	
	L	5,666,118	9/9/1997	Gersbach	341	120	
	M	5,710,563	1/20/1998	Vu et al.	341	161	
	N	5,790,060	8/4/1998	Tesch	341	119	
	O	5,825,317	10/20/1998	Anderson et al.	341	120	

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HN	P	Bastos, et al., "A 12-bit Intrinsic Accuracy High-Speed CMOS DAC", IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, December 1998, pp. 1959-1969.
	Q	Bugeja, et al., "A Self-Trimming 14-b 100-MS/s CMOS DAC", IEEE Journal of Solid-State Circuits, Vol. 35, No. 12, December 2000, pp. 1841-1852.
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	S	Diorio, et al., "A High-Resolution Non-Volatile Analog Memory Cell", IEEE, 1995, pp. 2233-2236.
	T	Diorio, "A p-Channel MOS Synapse Transistor with Self-Convergent Memory Writes", IEEE Transaction On Electron Devices, Vol. 47, No. 2, pp. 464-472, February 2000.
	U	SGS-Thomson Microelectronics, "An Overview of the Serial Digital Interface", 1994, pp. 1-28.

Examiner	HAI L. NGUYEN	Date Considered	06/07/2005

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	W	5,870,044	2/9/1999	Dell'ova et al.	341	120	
	X	5,870,048	2/9/1999	Kuo et al.	341	143	
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	AE	6,118,398	9/12/2000	Fisher et al.	341	148	
	AF	6,130,632	10/10/2000	Opris	341	120	
	AG	6,137,431	10/24/2000	Lee et al.	341	161	
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	AJ	6,191,715	2/20/2001	Fowers	341	120	
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HLN	AL	Tille, et al., "A 1.8-V MOSFET-Only Σ Δ Modulator Using Substrate Biased Depletion-Mode MOS Capacitors in Series Compensation", IEEE, Journal of Solid-State Circuits, Vol. 36, No. 7, July 2001, pp. 1041-1046.
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HLN	AN	Van der Plas, et al., "A 14-bit Instrinsic Accuracy Q^2 *Random Walk* CMOS DAC", IEEE Journal of Solid-State Circuits, Vol. 34, No. 12, December 1999, pp. 1708-1718.
HLN	AO	Vittoz, "Dynamic Analog Techniques", Design of MOS VLSI Circuits for Telecommunications, 1985, pp. 145-170.
HLN	AP	Vittoz, "Dynamic Analog Techniques", Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing, Chapter 4, 1994, pp. 97-124.
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